UNITED STATES PATENT AND TRADEMARK OFFICE

**UNITED STATES DEPARTMENT OF COMMERCE**
**United States Patent and Trademark Office**
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 11/502,488 | 08/10/2006 | Franz-Josef Menzl | 2005P11224US | 8216 |

22116 7590 10/17/2013

SIEMENS CORPORATION
INTELLECTUAL PROPERTY DEPARTMENT
170 WOOD AVENUE SOUTH
ISELIN, NJ 08830

| EXAMINER | |
|---|---|
| ITURRALDE, ENRIQUE W | |
| **ART UNIT** | **PAPER NUMBER** |
| 2179 | |
| **MAIL DATE** | **DELIVERY MODE** |
| 10/17/2013 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

---

BEFORE THE PATENT TRIAL AND APPEAL BOARD

---

*Ex parte* FRANZ-JOSEF MENZL, RALF MILDENBERGER, PABLO MUNOZ IBARRA, AXEL PLATZ, JOHANNA SCHMIDT, WILHELM WEHRFRITZ, and MARKUS WEINLANDER

---

Appeal 2011-009356
Application 11/502,488
Technology Center 2100

---

Before TONI R. SCHEINER, JEFFREY N. FREDMAN, and ULRIKE W. JENKS, *Administrative Patent Judges*.

FREDMAN, *Administrative Patent Judge*.

DECISION ON APPEAL

This is an appeal[1] under 35 U.S.C. § 134 involving claims to a system for graphical interconnection of a hardware signal of a controller device having a plurality of terminals. The Examiner rejected the claims as obvious. We have jurisdiction under 35 U.S.C. § 6(b). We reverse.

---

[1] Appellants identify the Real Party in Interest as Siemens Aktiengesellschaft (*see* App. Br. 1).

*Statement of the Case*

*Background*

The Specification teaches a "method with which a user can logically link hardware signals of a device, especially of a controller device, graphically to program elements in a simple manner, i.e. without having to know the address convention used in the system" (Spec. 2, ll. 15-18).

*The Claims*

Claims 10-12, 15, 17, 18, 24, and 25 are on appeal. Claim 10 is representative and reads as follows:

> 10. A system for graphical interconnection of a hardware signal of a controller device having a plurality of terminals, comprising:
>
> a processor unit for connection to the device, the processing unit having a keyboard and a mouse;
>
> a display device with a graphical user interface having a first area and a second area;
>
> a schematic presentation of the device in the first area, each device terminal displayed in accordance with a respective position on the device and provided with a logical address corresponding to an address convention used by the system to assign a hardware signal to the logical address; and
>
> a linking mechanism for logically linking the hardware signal assigned to the logical address with a program element of a programming environment presented in the second area,
>
> wherein a logical address of a terminal representation displayed in the first area corresponding to a hardware signal to be interconnected is selected, dragged, and dropped onto the program element, and
>
> wherein the dropped address is displayed with the program element in the second area, wherein a user-editable symbolic representation of the logical address is displayed together with the logical address, wherein the user-editable symbolic representation of the logical address is edited by clicking on the displayed terminal representation corresponding to the hardware signal to be

> interconnected, wherein the dropping of the representation of the selected terminal onto the program element causes the hardware signal to be logically linked via the logical address with the program element without a user having to know the address convention used by the system.

*The issue*

The Examiner rejected claims 10-12, 15, 17, 18, 24, and 25 under 35 U.S.C. § 103(a) as obvious over Anderson,[2] Molinari,[3] and Dardinksi[4] (Ans. 4-13).

The Examiner finds that Anderson teaches "a schematic presentation of the device in the first area . . . and a linking mechanism for logically linking the hardware signal assigned to the logical address with a program element of a programming environment presented in the second area" (Ans. 4). The Examiner finds that Anderson teaches "a logical address of a terminal representation displayed in the first area corresponding to a hardware signal to be interconnected is selected, dragged, and dropped onto the program element, and wherein the dropped address is displayed with the program element in the second area" (Ans. 4-5). The Examiner finds that Anderson also teaches "a user-editable symbolic representation of the logical address is displayed in the second area together with the logical address, wherein the user-editable symbolic representation of the logical address is edited with the graphical user interface" (Ans. 5).

---

[2] Anderson et al., U.S. 6,272,669 B1, issued Aug. 7, 2001.
[3] Molinari et al., U.S. 2003/0058280 A1, published Mar. 27, 2003.
[4] Dardinski et al., U.S. 6,754,885 B1, issued Jun. 22, 2004.

The Examiner finds that "Anderson fails to expressly disclose dragging and dropping, as recited in the claims" (Ans. 5). The Examiner finds that Molinari "describes dragging and dropping as a feature" (Ans. 5). The Examiner finds that "Anderson/Molinari fails to expressly disclose editing the representation by *clicking on the displayed terminal representation corresponding to the hardware signal to be interconnected*, as recited in the claim" (Ans. 6). The Examiner finds that "Dardinski discloses that a user may edit connections, parameters, block information and more by double clicking the compound/block name" (Ans. 6).

The Examiner finds it obvious to "modify the selecting, placing and connecting taught by Anderson to include dragging and dropping of Molinari, in order to obtain a dragging and dropping" (Ans. 6). The Examiner finds it obvious "to include dragging and dropping of Dardinski, in order to obtain a dragging and dropping. One would have been motivated to make such a combination to enter a new compound or block name, or select other parameters, as taught by Dardinski" (Ans. 6).

The issue with respect to this rejection is: Does the evidence of record support the Examiner's conclusion that Anderson, Molinari, and Dardinski render obvious a system "wherein a user-editable symbolic representation of the logical address is displayed together with the logical address, wherein the user-editable symbolic representation of the logical address is edited by clicking on the displayed terminal representation corresponding to the hardware signal to be interconnected" as required by claim 10?

*Findings of Fact*

1. Anderson teaches "a method for configuring a programmable semiconductor device using macros. A macro is a circuit block, sub-circuit block, or icon that contains configuration data to configure a programmable semiconductor device or a programmable circuit" (Anderson, col. 1, ll. 63-67).

2. Anderson teaches that the "process of designing an FPAA circuit in accordance with the present invention includes selecting, placing, and connecting a plurality of macros in a work area. When a macro is placed and connected in a work area, the configuration data of the macro is combined with the configuration data of the work area" (Anderson, col. 5, ll. 26-31).

3. Anderson teaches that "[s]hortcut area **26** has a macro selection area **38** and a line connection area **39**. Macro selection area **38** displays a plurality of macros from a macro library when selected or contacted by a selection device" (Anderson, col. 2, l. 65 to col. 3, l. 1).

4. Anderson teaches that "[l]ine connection area **39** is used to make connections between global lines, the terminals of macros, and the terminals of I/O blocks when selected by a selection device" (Anderson, col. 3, ll. 1-3).

5. Anderson teaches:

> A connection tool **56** is displayed by contacting line connection area **39** (FIG. **3**). A first terminal of a connection line **57** is connected to terminal **33**C of I/O block **22**C using connection tool **56**. Status area **27** dynamically displays a plurality of text messages to signal valid connections and connection restrictions within work area **10**. In other words,

> the plurality of text messages displayed in status area **27** continuously signal whether a connection with connection tool **56** can or cannot be made and the reason a connection cannot be made at a particular point within work area **10**.

(Anderson, col. 3, ll. 35-45).

6. Molinari teaches that:

> By selections from menu lists, or the "drag and drop" of selected panel icons presented in "flying tool windows", the user places on the design workspace a selection of "panels", chosen to represent the several instrument components that will need to be combined to form an "instrument" of the kind required by the user's intended application.

(Molinari 3 ¶ 0025).

7. Dardinski teaches

> The user can perform different functions on different parts of the Block Placeholder by right-clicking to bring up the context menu. Context menus contain unique functions depending on the object on which they are invoked. For example, the user has the option to edit connections, parameters, block information, etc. The default double-click function for the Compound/block name section is to prompt for new Compound and Block Names. The default function for the source/sink parameters sections is to bring up a connection dialog. In the Relevant block parameters section, the default action is to select parameters displayed from a list of block parameters. The default action for the center of a block is to bring up the block's Property Sheet.

(Dardinski, col. 79, ll. 52-64).

8. The Specification teaches that "a symbolic name can be allocated in each case to the terminals in the schematic presentation of the device, and this name can be displayed together with the logical address of

the relevant terminal in the programming environment" (Spec. 4, l. 34 to 5, l. 2).

9. The Specification teaches that the "name is edited directly at the terminal by clicking on the representation of a hardware signal in the schematic presentation. The simultaneous presentation of the symbolic name and the logical address is an additional simplification for the user in learning the address convention used in the engineering system" (Spec. 5, ll. 2-7).

*Principles of Law*

"The protocol of giving claims their broadest reasonable interpretation during examination does not include giving claims a legally incorrect interpretation. This protocol is solely an examination expedient, not a rule of claim construction." *In re Skvorecz*, 580 F.3d 1262, 1267 (Fed. Cir. 2009).

*Analysis*

Appellants contend that "[n]owhere the Examiner points out with specificity, which element of Anderson in FIGs. 1, and 3-7 of Anderson is being construed as the logical address and which element of Anderson is being construed as the user-editable symbolic representation of the logical address" (App. Br. 7). Appellants contend that "[n]either Molinari nor Dardinski cures the foregoing deficiency of Anderson in connection with the claimed invention" (App. Br. 8).

The Examiner responds that:

> Anderson teaches the limitations in question using Figures 4-5 and 7. Specifically, Anderson describes wherein the dropped address is displayed with the program element in

> the second area *by teaching selecting, placing and connecting of components (see lines 26-44 of column 5 and Figure 7)*, wherein a user-editable symbolic representation of the logical address is displayed in the second area together with the logical address *by teaching input and manipulations of parameters (see lines 60-67 of column 3 and lines 1-37 of column 4).*

(Ans. 14). The Examiner finds that a "user-editable symbolic representation of the logical address appears to be a broad term of the limitation. It is understood to be a representation that symbolizes a logical address and may be edited by a user. How the representation may be edited and what the representation consists of is open to broad interpretation" (Ans. 15). The Examiner finds that "[e]diting may be performed by connecting lines to the representation to display an existing connection at the address" (Ans. 15).

We find that Appellants have the better position. While we interpret claims using the broadest reasonable interpretation in light of the Specification standard, the interpretation must be reasonable. The Specification teaches that a symbolic name of a terminal, associated with the "logical address of the relevant terminal", is capable of being edited by a user (FF 8-9), so the ordinary artisan would reasonably interpret this phrase as minimally permitting editing of a symbolic name associated with a terminal.

The portions of Anderson identified by the Examiner at columns 3-5 provide no teaching or suggestion of a "user-editable symbolic representation" as required by claim 10, with no teaching of any user-editable name whatsoever. Indeed, the word "edit" was not found in Anderson using a word search of the text.

We are also not persuaded by the Examiner's argument that "[e]diting may be performed by connecting lines to the representation to display an existing connection at the address" (Ans. 15). We are not persuaded that the Examiner's reliance on the connecting lines, which may be dragged and dropped by the user, reasonably satisfies the claim requirement for a "user-editable symbolic representation of the logical address." In Anderson, the connecting lines do not function as a symbolic representation of any type of address, but simply serve to show the connection between terminal 33C to 53A. They lines are very different than a logical address, which is reasonably understood as information which defines the specific location of a particular terminal or signal within the larger device (*see* Spec. 1, ll. 16-30). They are also different than a symbolic address, which permits the user to give hardware "names which convey a certain meaning to the user" (Spec. 1, ll. 35-36).

The lines in Anderson represent neither logical addresses, which define a particular location of a particular terminal, nor symbolic addresses, which are user defined addresses that define the location of a particular terminal, but Anderson's lines instead represent connections between two terminals. Therefore, the interpretation of the lines as satisfying the "user-editable symbolic representation" limitation is not found persuasive.

*Conclusion of Law*

The evidence of record does not support the Examiner's conclusion that Anderson, Molinari, and Dardinski render obvious a system "wherein a user-editable symbolic representation of the logical address is displayed together with the logical address, wherein the user-editable symbolic

representation of the logical address is edited by clicking on the displayed terminal representation corresponding to the hardware signal to be interconnected" as required by claim 10.

## SUMMARY

In summary, we reverse the rejection of claims 10-12, 15, 17, 18, 24, and 25 under 35 U.S.C. § 103(a) as obvious over Anderson, Molinari, and Dardinksi.

## REVERSED

lp